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(54) Switching method for a common memory based switching field and the switching field.

(57) The invention pertains to a switching method for a common memory based switching field and to the switching field. In the method (1) a plurality of input gates ($a_1 ... a_n$) receive cells (10), each comprising a header (11) and a payload portion (12); (ii) the header (11) and the payload portion (12) of a cell (10) arriving at the switching field are separated from each other, whereby header conversion operations required for the next link are performed in respect of the header (11), and the payload portion (12) is written to a common memory (24); (iii) and each cell (10) is transmitted via one or more output gates ($c_1 ... c_n$) to one or more output lines. In order to optimise practical apparatus for obtaining a faster switching time and, as a result, a larger number of gates for each switching block, packets consisting of a new header obtained from the header conversion and a common memory address of the payload are switched to a time-shared bus (22) which routes each packet to output buffers ($b_1 ... b_n$) in a manner known per se; and when each cell is to be transmitted, a corresponding payload portion (12) is read from the common memory (24), said payload portion (12) and said new header are combined into a new cell, and the new cell is transmitted to said one or more output lines.

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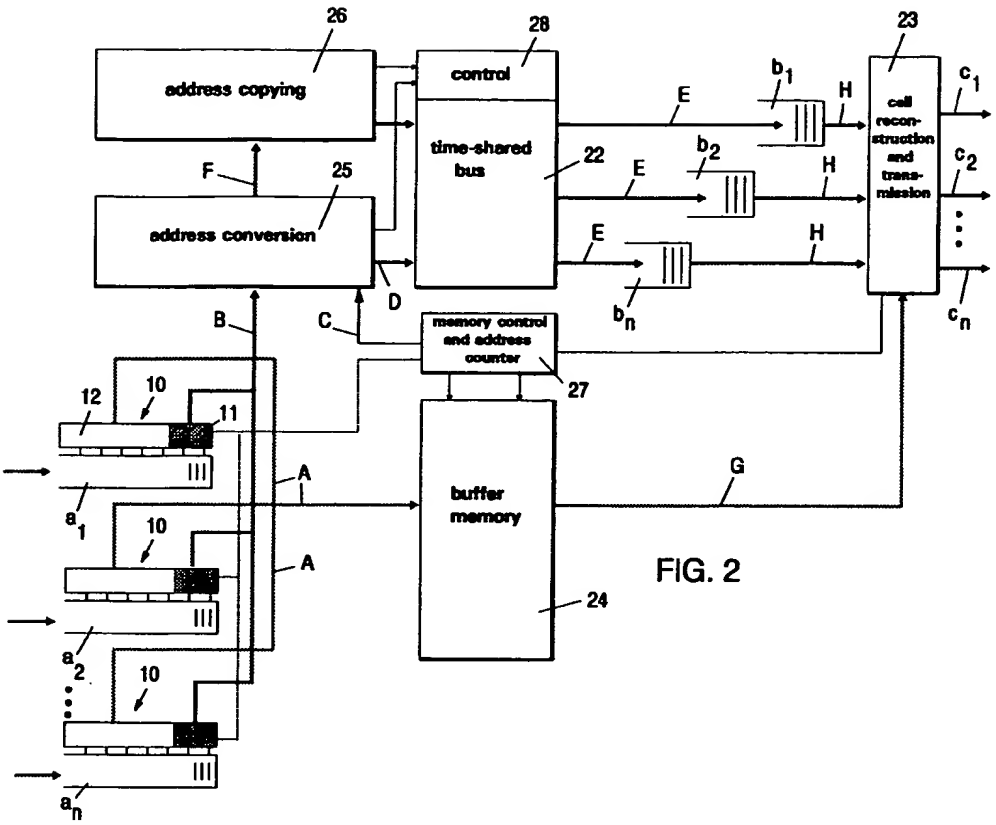
26
address copying
28
control
time-shared bus
22
23
cell reconstruction and transmission
F
25
address conversion
D
E
H
b_1
b_2
b_n
c_1
c_2
c_n
B
C
memory control and address counter
27
12
10
11
A
buffer memory
24
G
a_1
a_2
a_n

FIG. 2

The present invention pertains to a switching method for a common memory based switching field and to the switching field. In the method (i) a plurality of input gates receive cells, each comprising a header and a payload portion; (ii) the header and the payload portion of a cell arriving at the switching field are separated from each other, whereby the header conversion operations required for the next link are performed in respect of the header, and the payload portion is written to a common memory; and (iii) each cell is transmitted via one or more output gates to one or more output lines.

The need for broadband information transfer constantly increases in public networks. The high speed of a broadband integrated services network, such as B-ISDN (Broadband Integrated Services Digital Network), where voice, image and text are transferred, requires an effective and simple network protocol. The Asynchronous Transfer Mode (ATM) is generally considered the best alternative, because it enables transmission of both interactive and distribution services at the maximal transmission rate of the network or at any lower rate. The asynchronous mode is based on asynchronous time division channelling, in which information is transferred in packets of predetermined length, called cells. Owing to the above features, the preferred embodiment of the present invention is an ATM switching field.

The independently functioning basic part of an ATM switching field is a switching block, which carries out the actual switching. By increasing the size of one switching block in the switching field, the number of switching blocks required in the switching field may be reduced, and the apparatus may thus be made simpler. Owing to high transmission rates, one switching block must however be very fast. In common memory based switching fields, the size of a switching block is limited by the speed of writing to and reading from the memory. In the worst case, one cell is to be written to the common memory from each input line and one cell to each output line during the time taken for one cell to arrive from the input line.

The description of the prior art in U.S. patent 4,947,388 sets forth an ATM switching field which, similarly to the present invention, is based on a common memory and which comprises 32 input lines and 32 output lines. Each incoming ATM cell is divided into a header and a payload portion. The payload portion is written to a buffer memory storage location corresponding to the input line. The header is applied to a conversion circuit, which gives the routing information of the header, e.g. the number of the output line and the logical channel number. The latter is obtained from the output of the conversion circuit synchronised with the writing of the payload portion to the memory, and is written to the buffer memory together with the payload portion. The address of the buffer memory where the payload portion and the logical channel number are written is applied to a group of 32 output queues and stored into one of these (into the queue indicated by the conversion circuit). Each output queue corresponds to one output line, and the payload portions and logical channel numbers (cells) corresponding to the output lines are read successively from the buffer memory, from storage locations indicated by the output queues. From the output of the buffer memory (where the cells are in multiplex form) the cells are switched via a demultiplexor to their own output lines.

The drawback of the above switching field structure relates to the speed problem described above. Since the logical channel number is written to the buffer memory together with the payload portion, the payload portion has to wait the time of the header conversion before it may be stored into the buffer memory. This shortens the time available for writing cells to the memory, whereby the largest possible number of gates is reduced. Alternatively, the solution requires longer buffering of the cells before writing to the memory, which in turn increases the quantity of apparatus and the delay caused by the field.

The object of the present invention is thus to optimise the practical devices so that an improved result is achieved with the existing technique, in other words a faster switching time and, consequently, a larger number of gates for a switching block. This is achieved with the method of the invention, which is characterised in that packets consisting of a new header obtained from the header conversion and a common memory address of the payload are switched to a time-shared bus which routes each packet to output buffers in a manner known per se, and that when each cell is to be transmitted, a corresponding payload portion is read from the common memory, said payload portion and said new header are combined into a new cell, and the new cell is transmitted to said one or more output lines. The switching field of the invention for its part is characterised by what is described in the characterising portion of accompanying claim 3.

The basic concept of the invention is to use distributed switching between the time-shared bus and the common memory, in such a manner that the switching itself is carried out with a packet which is considerably shorter than a normal ATM cell and which consists of the new header of the cell and the common memory address of the payload portion, by means of a time-shared bus, whereby writing of the payload portion of the cell to the common memory is carried out concurrently

with the header operations and the switching, and that the cell will be reconstructed when it is to be transmitted to the output line.

The solution of the invention speeds up the switching, and this increases the largest possible number of gates. The time-consuming handling of the header separate from the common memory increases the time available for writing to the common memory, which also increases the largest possible number of gates. As an alternative to increasing the number of gates, the parallelism may be reduced, which often makes the practical solution simpler.

Since the solution utilises the common memory, the required number of block buffers is reduced. Even though the switching field of the invention is logically output-buffered, the required number of buffers is not large: since the payload portion is separate in the common memory, short packets are buffered in the output (approx. 15% of an entire ATM cell).

Carrying out the header operations of the cell in parallel with the writing of the payload to the common memory also reduces the delay caused by the switching field, and this reduces the need for buffering. Shortening of the delay is essential when interactive services such as a video conference or high-quality viewphone service are to be provided.

In the following the invention and its preferred embodiments are described in more detail with reference to the examples of the accompanying drawing wherein

Figure 1 shows the structure of an ATM cell, and

Figure 2 is a block diagram of an ATM switching field of the invention.

An ATM cell 10 illustrated in Figure 1 consists of a header 11 and a payload portion 12. The header is specific for each link, and it indicates e.g. the virtual channel and bus to be used. When a cell is transmitted via the switching field to another connection, it must be designated a new header, which is assigned for said new connection. The cell, as well as the header and payload portion contained therein, are each of fixed length, but the measures may vary from one system to another. The Consultative Committee for International Telephone and Telegraph, CCITT, has however agreed that the header has a length of 5 bytes and the payload portion a length of 48 bytes.

Figure 2 is a block diagram of an ATM switching field of the invention. The field comprises n input gates $a_1 ... a_n$, each comprising a specific input buffer. ATM cells 10 of Figure 1 arrive from the input lines at the input gates in a manner known per se. The input gates are connected to both a time-shared bus 22 and a common memory 24 which is connected in parallel with said time-shared bus. Said time-shared bus 22 carries out routing to output buffers $b_1 ... b_n$,which are connected via a reconstruction circuit 23 to output gates $c_1 ... c_n$. The use of a time-shared bus as a switching block is known per se and described e.g. in references [1] and [2] (a list of references can be found at the end of the specification). Switching from the input gates to the time-shared bus 22 takes place via a header conversion circuit 25, and in the case of distribution traffic (described further below), also through an address-copying circuit 26. In addition, the switching field comprises a memory control and address counter circuit 27. The control element of the time-shared bus is also illustrated as a separate block, indicated by the numeral 28.

A normal switching (point-to-point) is performed in the switching field as follows. When the ATM cell 10 arrives at one of the input gates, said memory control and address counter circuit 27 contains an indication of available storage locations of the common memory 24. At said input gate the payload portion 12 is separated from the cell 10 and is written, controlled by said circuit 27, to an available storage location of the common memory 24. This operation is illustrated by arrows A. Handling of the header 11 of the cell is started simultaneously with the writing to the memory by applying the header (arrows B) to the header conversion circuit 25, where the known address conversion required for the next link and other possible header operations known per se are performed in respect of the address of the header. The common memory address of the payload portion obtained from the memory control and address counter circuit 27 is added to the new header thus obtained (arrow C). A packet consisting of the new header and said common memory address is written to the input of the time-shared bus 22 (arrow D). The time-shared bus 22 routes said packet in a manner known per se (c.f. e.g. reference [1]) to an output buffer b1...bn (arrows E) corresponding to the output line in question. When said cell is to be transmitted, the corresponding payload portion 12 is fetched from the common memory 24 on the basis of the common memory address (arrow G) and the corresponding new header is fetched from the output buffer to the reconstruction circuit 23 (arrows H). In the reconstruction circuit the new header and the payload portion are reconstructed as a new ATM cell, and said cell is written to the corresponding output line via an output gate determined by the new header. The reconstruction of the cell thus takes place in connection with the transmission of said cell.

Routing of a packet consisting of the header of an ATM cell and the memory address of the payload is considerably faster than routing of a com-

plete, clearly longer ATM cell. This increases the largest possible number of gates. Alternatively, the number of parallel operations may be reduced, which makes the practical realisation simpler.

Distribution traffic (copying of cells, point-to-multipoint) takes place in such a manner that in connection with the header conversion the header is discovered by the header conversion circuit 25 to belong to a distribution connection (1 bit in the conversion table). As a result, the header is written to an address-copying circuit 26 (arrow F), which performs the same operations as the header conversion circuit, yet so that a plurality of outgoing addresses are made from one incoming address, all containing a reference to the same common memory address. The packets of the distribution traffic are guided to the time-shared bus 22 when the header conversion circuit 25 has no header to offer or the header handled by it is intended for the address-copying circuit.

Even if the invention was described in the foregoing with reference to the example illustrated by the accompanying drawing, it is clear that the invention is not limited thereby but may be modified in many ways within the scope of the inventive concept disclosed above and in the enclosed claims. Therefore, even if the above example concerns an ATM switching field, a similar concept may be used in conventional packet-switching systems as well. The ATM-specific terms used are thus to be understood in a larger sense. For instance, by a cell is meant in a more general sense a packet.

References cited:

[1] De Prycker M., Bauwens J.: A Switching Exchange for an Asynchronous Time Division based Network, International Conference on Communications 1987, 7-10 July 1987, Seattle, Washington, USA, p. 774-781

[2] Pöntinen Juha: Switching network structure in the Broadcast Integrated Services Digital Network. Master's thesis, University of Technology, Laboratory of Telecommunication Switching and Information Technology, Espoo 1989.

Claims

1. A switching method for a common memory based switching field, wherein
   - a plurality of input gates ($a_1 ... a_n$) receive cells (10), each comprising a header (11) and a payload portion (12);
   - the header (11) and the payload portion (12) of a cell (10) arriving at the switching field are separated from each other, whereby header conversion operations required for the next link are performed in respect of the header (11), and the payload portion (12) is written to a common memory (24); and
   - each cell (10) is transmitted via one or more output gates ($c_1 ... c_n$) to one or more output lines, **characterised** in that packets consisting of a new header obtained from the header conversion and a common memory address of the payload are switched to a time-shared bus (22) which routes each packet to output buffers ($b_1 ... b_n$) in a manner known per se, and that when each cell is to be transmitted, a corresponding payload portion (12) is read from the common memory (24), said payload portion (12) and said new header are combined into a new cell, and the new cell is transmitted to said one or more output lines.

2. A method according to claim 1, **characterised** in that a packet consisting of the new header obtained by the header conversion and the memory address of the payload (12) is switched to the time-shared bus (22) from an address-copying circuit (26) where copying of one incoming address into a plurality of addressess is performed in addition to the header conversion operations, whereby a plurality of packets, all having the same common memory address, are switched to the time-shared bus (22) for one incoming cell.

3. A switching field comprising
   - a plurality of input gates ($a_1 ... a_n$), which receive cells (10), each comprising a header (11) and a payload portion (12);
   - a plurality of output gates ($c_1 ... c_n$), through which said cells are transmitted to one or more output lines;
   - header conversion means (25) for conversion of the header (11) of an incoming cell (10) for the next link; and
   - a common memory (24) for storing the payload portion (12) of the cell (10), **characterised** in that a known time-shared bus (22) is connected in parallel with said common memory (24) so that packets consisting of a header converted for the next link of the cell and a common memory address of the payload (12) are routed therethrough to output buffers ($b_1 ... b_n$), and that the switching field comprises means (23) connected with the output buffers for combining said converted header and payload portion (12) of the cell and subsequently

transmitting to one or more output lines.

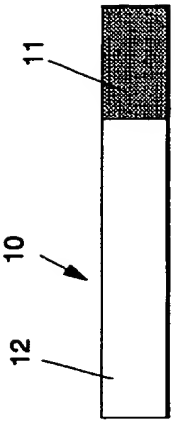
11
10
12

FIG. 1

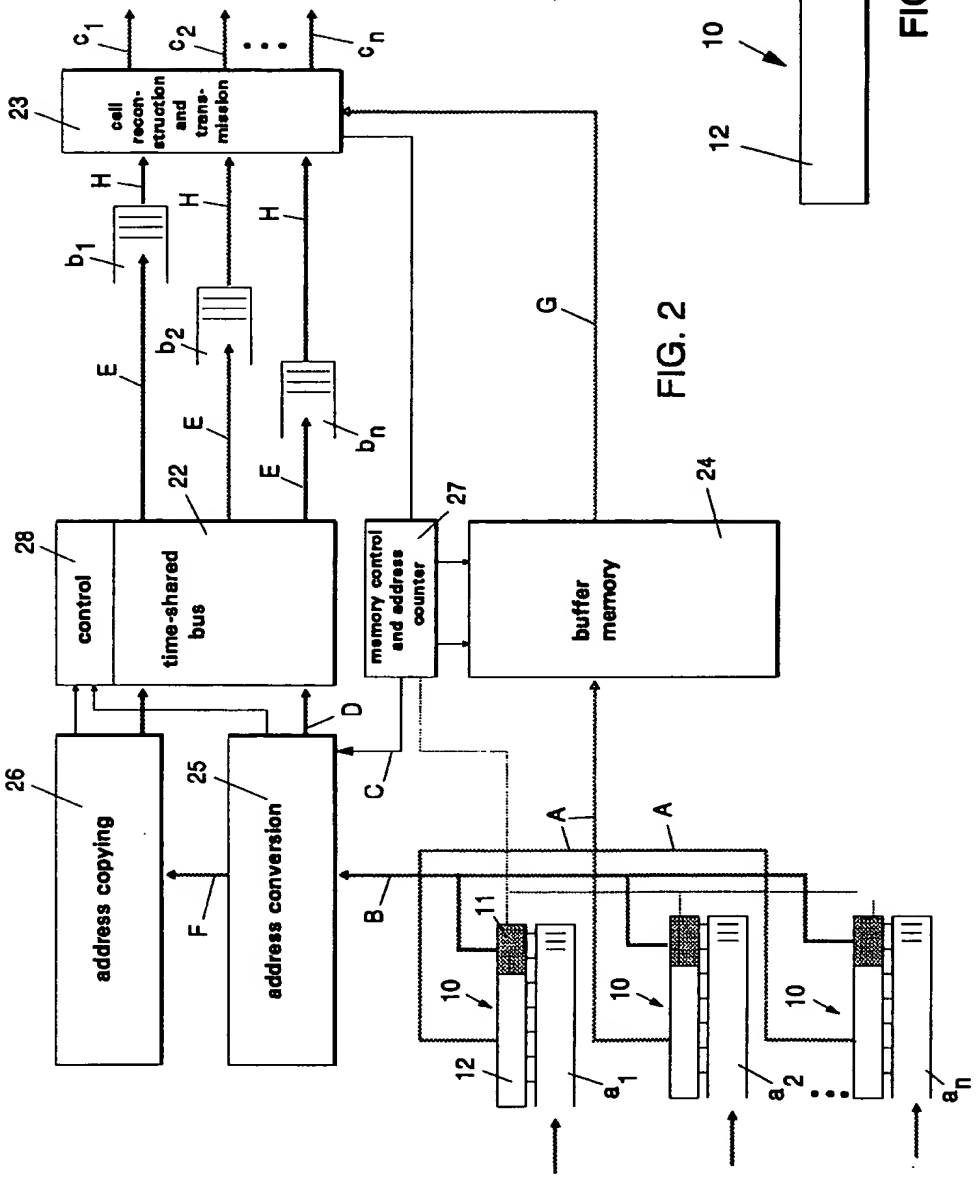
23
cell reconstruction and transmission
c_1
c_2
c_n
H
b_1
b_2
b_n
E
G
22
time-shared bus
control
28
27
memory control and address counter
24
buffer memory
D
C
26
address copying
25
address conversion
F
B
A
11
10
12
a_1
a_2
a_n

FIG. 2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 11 7638

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS vol. 6, no. 9, December 1988, US pages 1528 - 1537 , XP112418 M. DEVAULT ET AL * SECTION IV. B. *	1-3	H04L12/56 H04Q11/04
A	EP-A-0 338 558 (NEC) * column 12, line 10 - line 55 *	1,3	
A	INT. SWITCHING SYMPOSIUM 90 vol. 5, May 1990, SE pages 1 - 8 , XP130918 M. HENRION ET AL * SECTION 5.4 *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H04L H04Q

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 FEBRUARY 1993	A. ALI

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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